

FIGURE 1

250

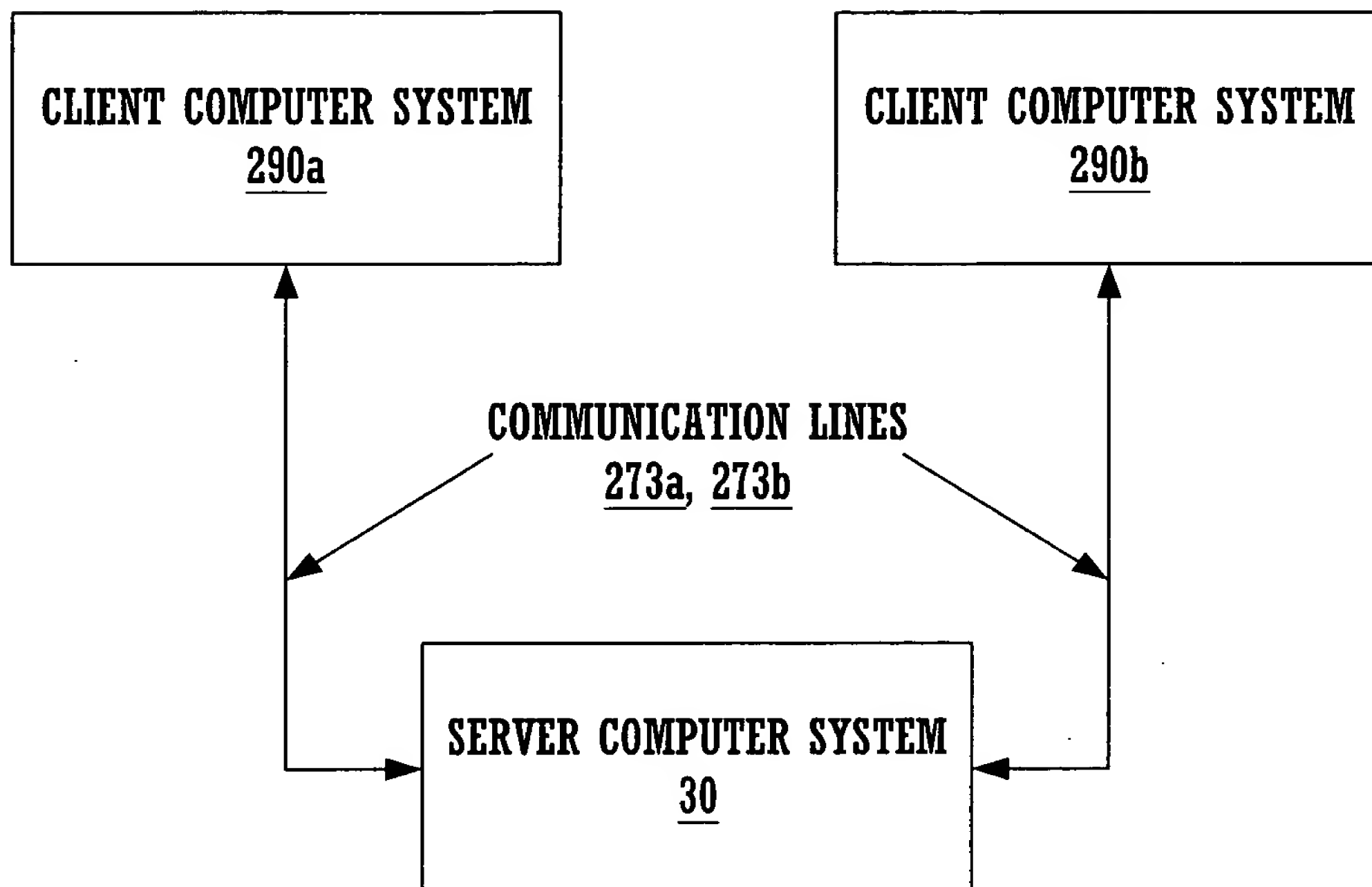


FIGURE 2

300

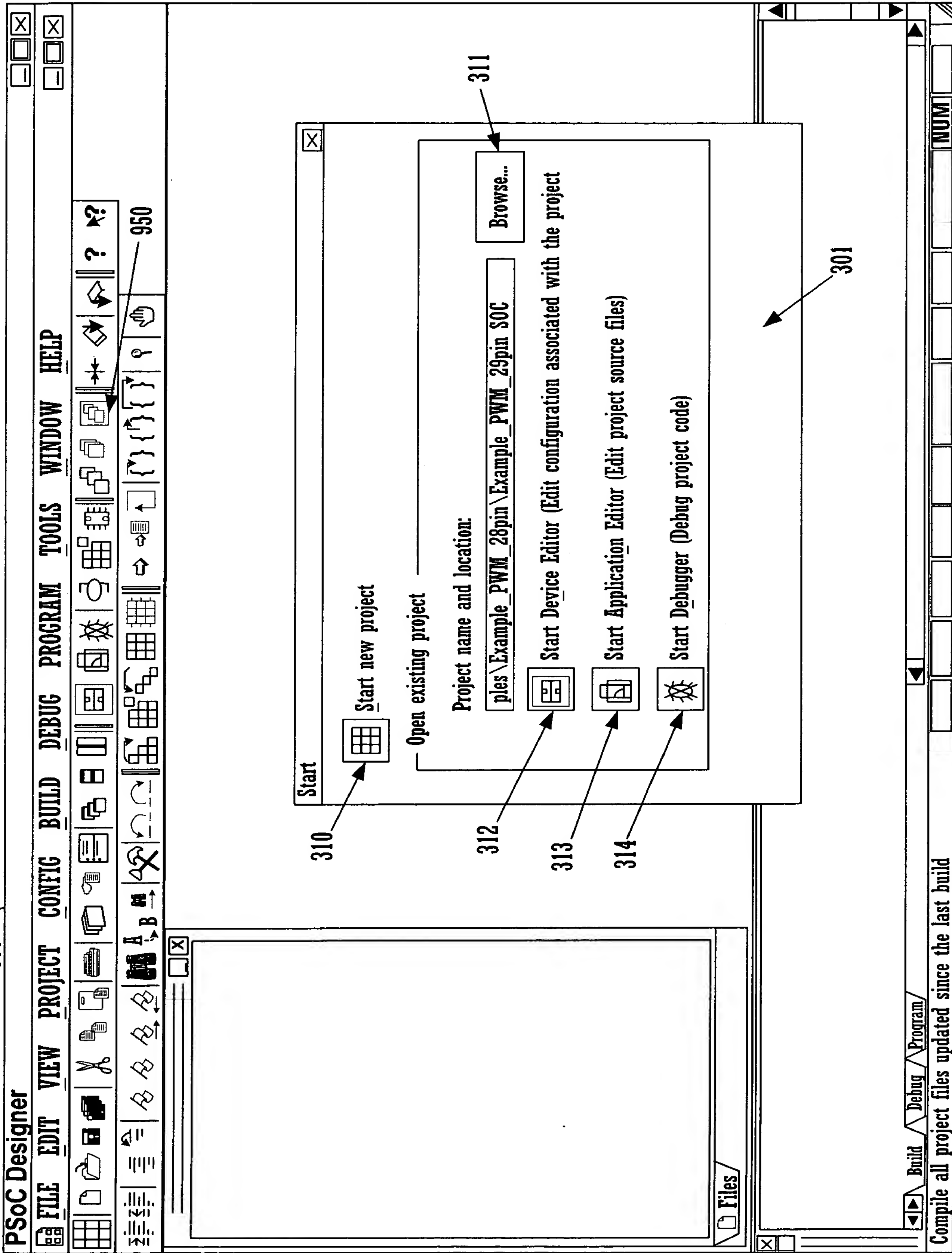


FIGURE
3

400

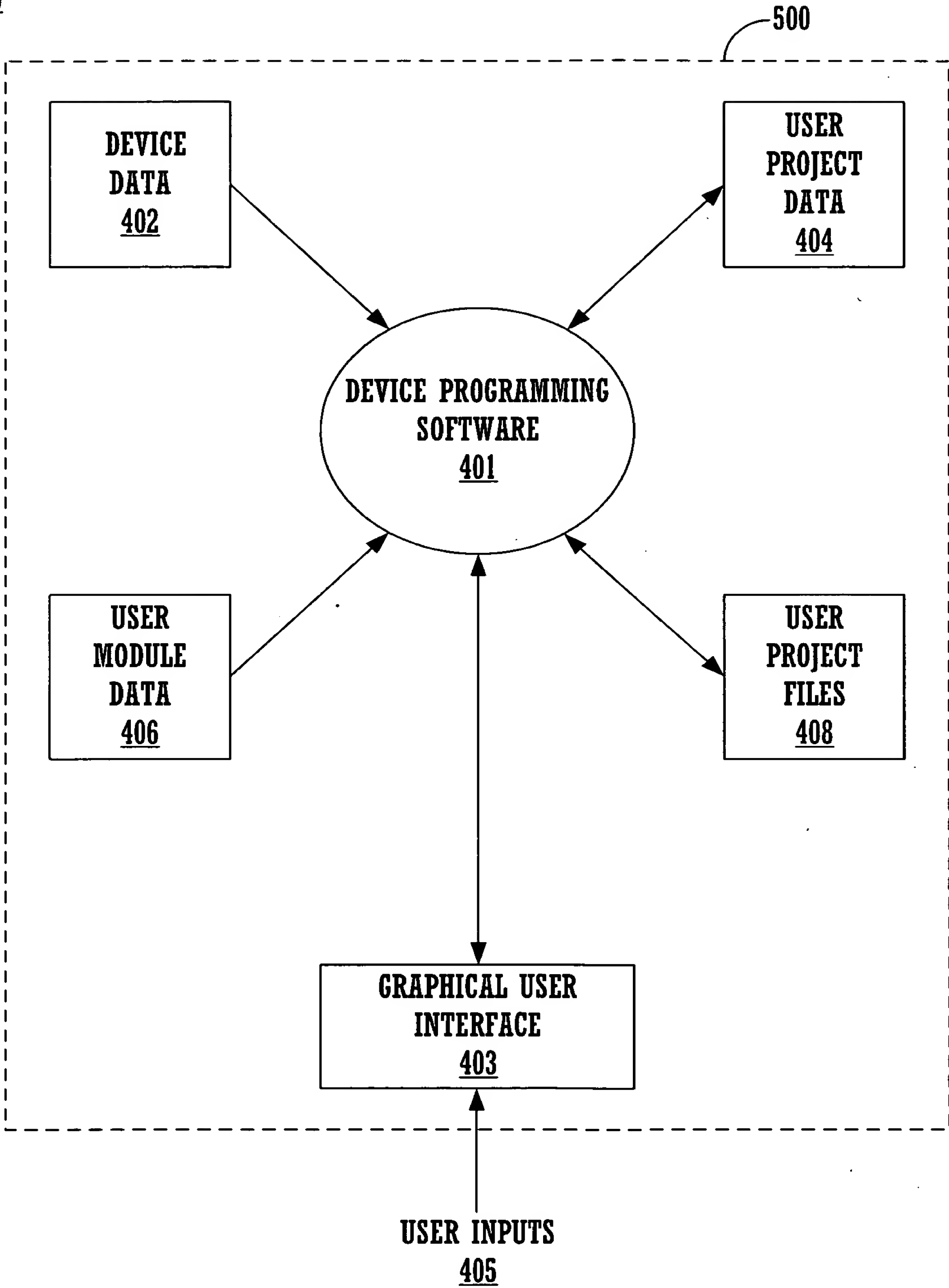


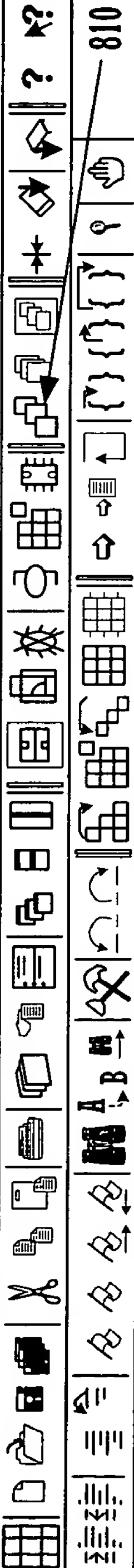
FIGURE 4

Replacement sheet

500

Test PSoC Designer [Device Editor]

FILE EDIT VIEW PROJECT CONFIG BUILD DEBUG PROGRAM TOOLS WINDOW HELP



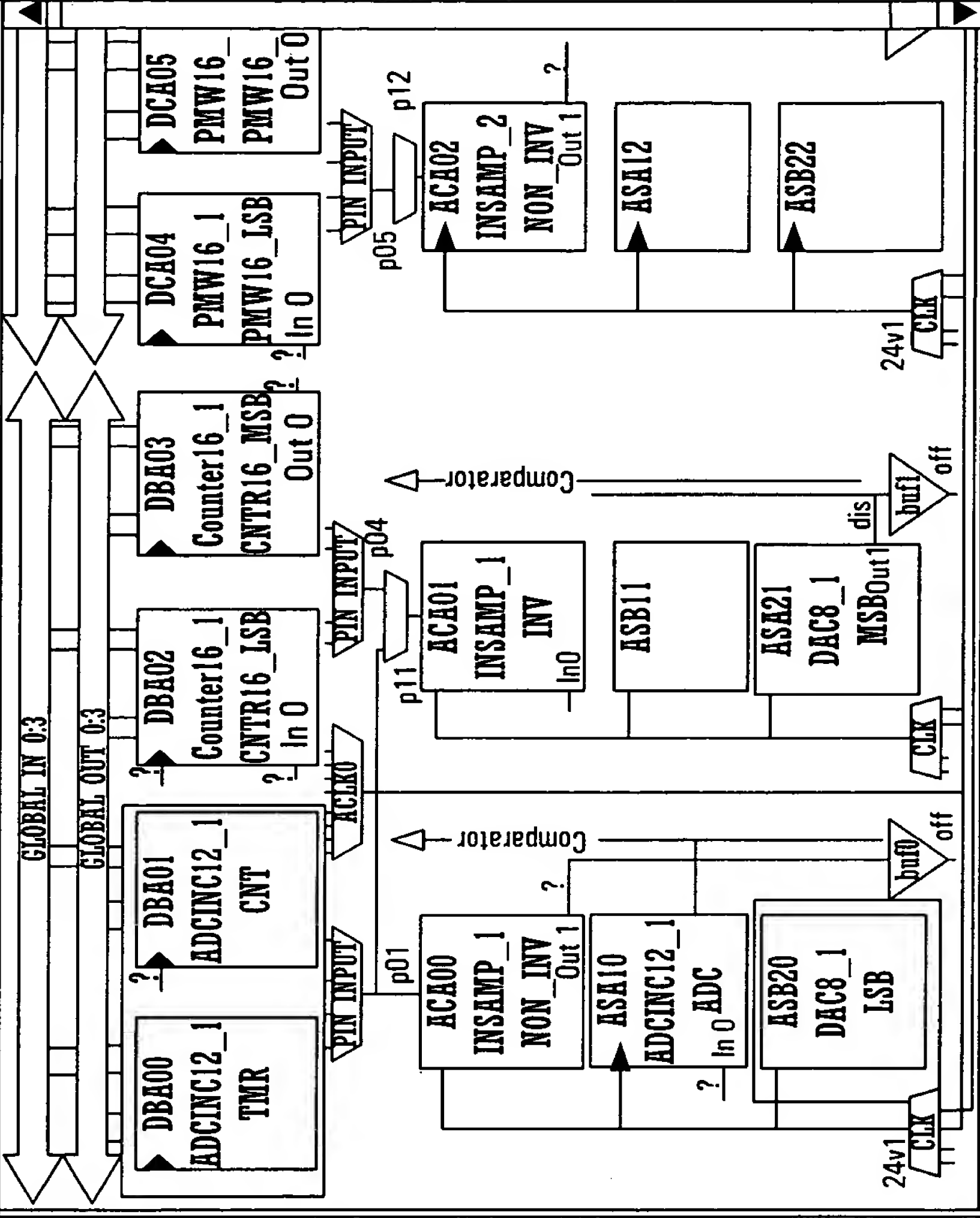
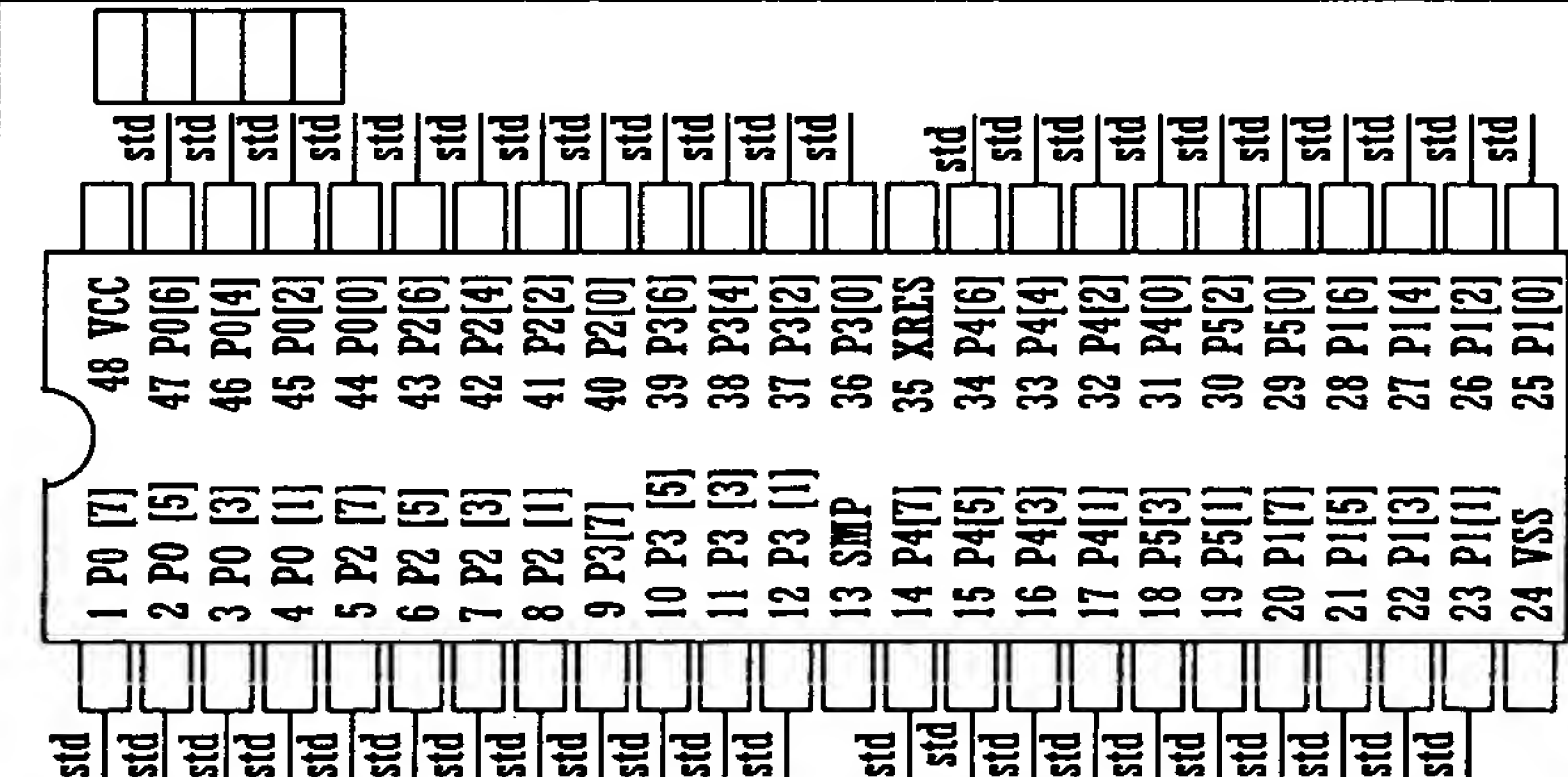
Global Resources

CPU_Clock 3_MH
32K_Select Interna
PLL_Mode Disable
Sleep_Timer 512_H
24V1=24MHz/N 1
24V2=24V1/N 1
Analog Power SC On/
Ref Mux (Vcc/2)
Op-Amp Bias Low
A_Buff_Power Low
SwitchModePump Off
VoltMonRange 5.0V
VoltMonThreshold 80%

USER MODULES SELECTED FOR PLACEMENT

ADCINC12_1 Counter16_1 DAC8_1

INSAMP_1 INSAMP_2 PWM16_1 UART_1



For Help, press F1

NUM

FIGURE 8

900

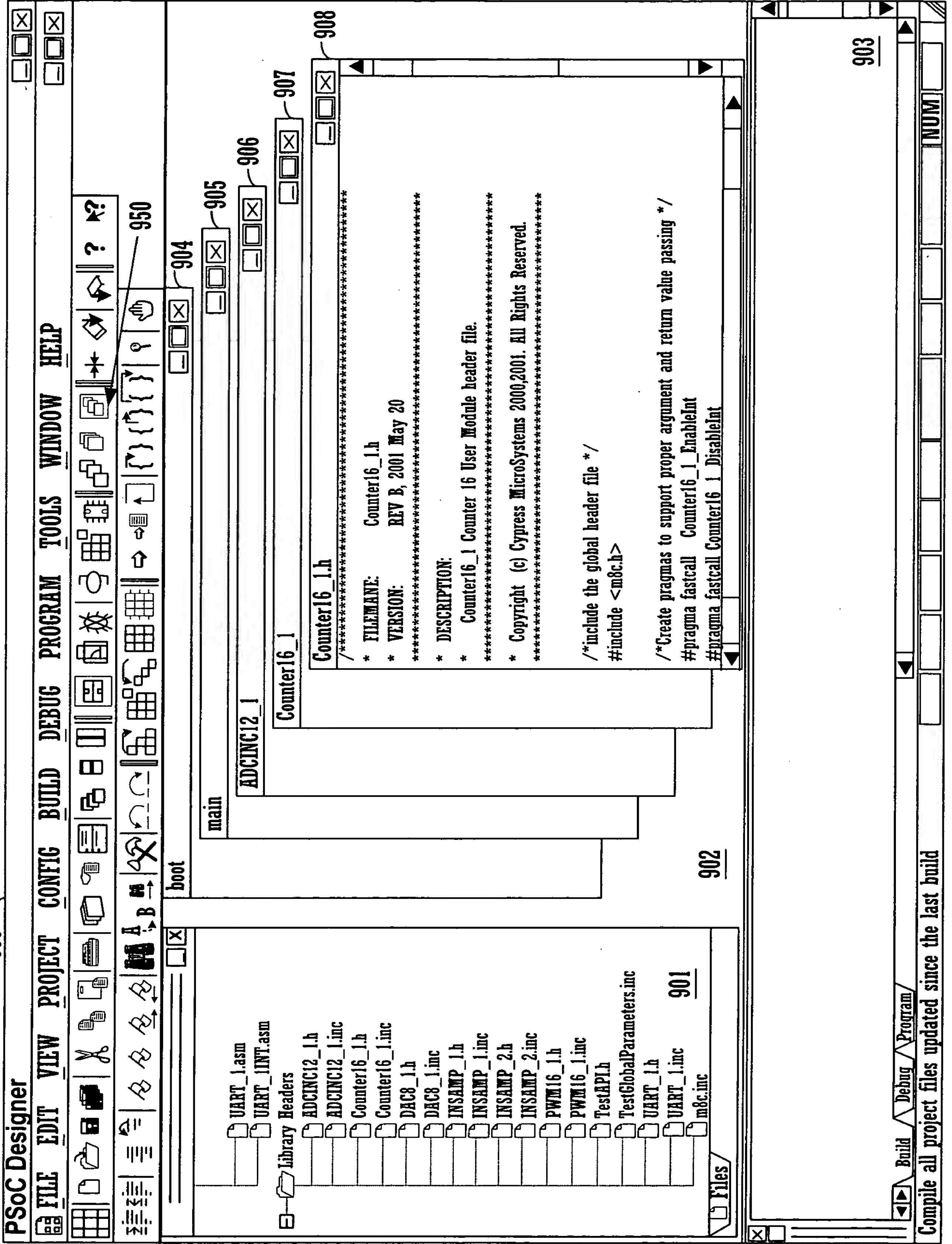


FIGURE
9

11/11

1000

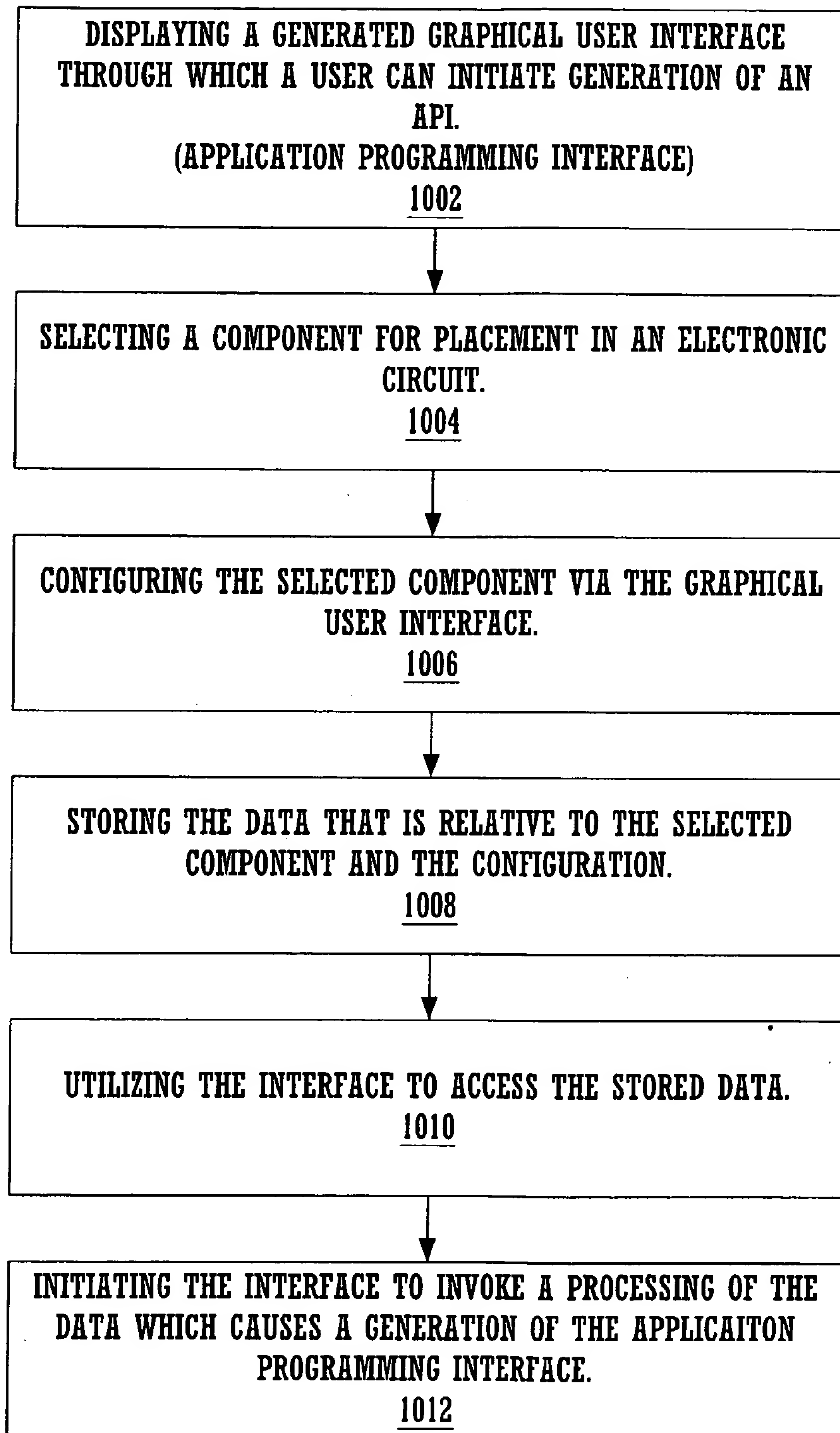


FIGURE 10